

## **Experiments for Basic Characteristics of OP AMP**

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# **14**

- 14.1 Study Objective
- 14.2 Basic Description
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## Chapter 14 Experiments for Basic Characteristics of OP AMP

### 14.1 Study Objective:

- (1) Understanding the basic characteristics of OP AMP.
- (2) Understanding the adjustment method for offset voltage of OP AMP.

### 14.2 Basic Description:

#### 14.2.1 New Terminology:

(1) Offset:

When  $V_i$  of OP AMP is 0V,  $V_o$  shall be 0V in the ideal case. However, because of the imbalance in the internal circuits of the OP AMP,  $V_o$  is usually drifted from 0V. This drifting status exhibits an output offset voltage ( $V_{os}$ ) at the output terminal. This  $V_{os}$  can be offset to 0V if an effective voltage is applied in the input terminal. This adjustment for turning  $V_{os}$  into 0V using this concept is the offset voltage adjustment which will be described in Experiment 14-2 Item (5) (6).

(2) CMRR (Common Mode Rejection Ratio):

Common Mode Rejection Ratio can be expressed as CMRR or  $\rho$ .  $\rho = A_d / A_c$ , the value of which shall as larger as possible.

#### 14.2.2 Basic Principle:

14-1 Transistor differential amplifier circuit

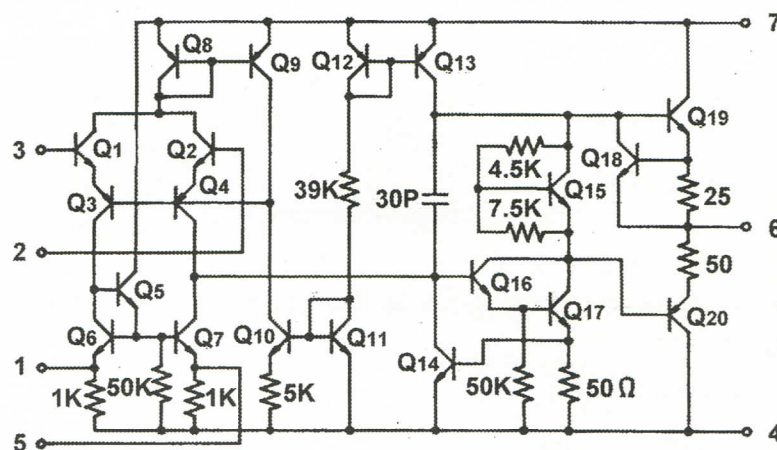
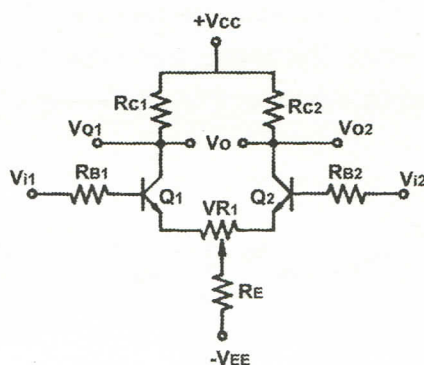
The internal equivalent circuit of a practical OP AMP ( $\mu A$ ) is shown in Fig 14.1, wherein its circuit structure is similar to OCL AMP, with differential amplification configuration in the input stage. We will briefly analyze the properties of differential amplifier as follows.

## (1) Structure of differential amplifier circuit

Fig 14.2 (a) shows the circuit which is composed of two CE amplifiers with common emitter resistor, two input terminal  $V_{i1}$ ,  $V_{i2}$ , and two output terminals  $V_{o1}$ ,  $V_{o2}$ . The complete internal circuit of a differential amplifier IC is shown in Fig 14.2 (b), with circuit symbol shown in Fig 14.2 (c). The output signal of the differential amplifier is the amplified magnitude of the difference between two input signals. In other words, the output signal is directly proportional to the difference between two input signals:  $V_o = A_v (V_{i1} - V_{i2})$ .

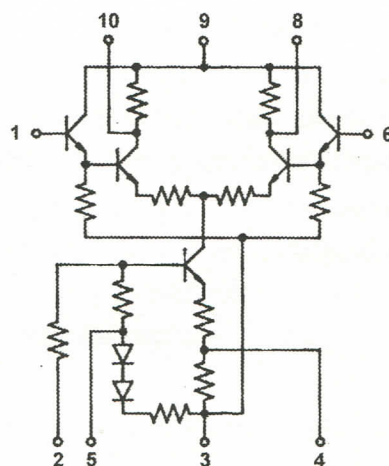
## (2) Input/Output configurations of differential amplifier

- 1) Single-end input, single-end output.
- 2) Single-end input, dual-end output.
- 3) Dual-end input, single-end output.
- 4) Dual-end input, dual-end output.

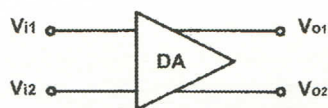
Fig 14.1 Internal equivalent circuit of  $\mu A741$ 

(a) Basic circuit





(b) Internal circuit of the IC



(c) Symbol

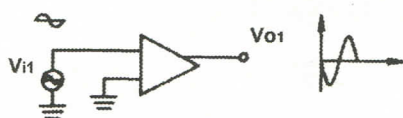
Fig 14.2 Differential amplifier

We will analyze the input/output configurations of the differential amplifier as follows:

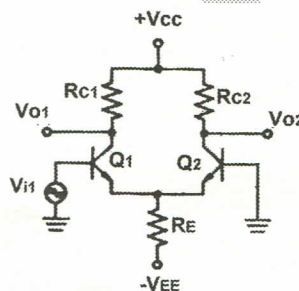
1) Single-end input, single-end output

1.  $V_{o1}$

As shown in Fig 14.3 (a) (b), because Q1 is arranged as the CE amplifier,  $V_{i1}$  is fed to base then is amplified, and the output is taken from the collector. According to the characteristics of CE amplifier -- the output signal from the collector is in inverse phase with the input signal of base, the output signal  $V_{o1}$  of Q1 is in inverse phase with  $V_{i1}$ . In other words, the phase difference between input and output is  $180^\circ$ , which can be expressed as  $V_{o1} = -A_v V_{i1}$ .



(a)



(b)

Fig 14.3 Single-end input, single-end output (I)



## 2. Vo2

As shown in Fig 14.4 (c), when the  $V_{i1}$  signal is feeded into the base of Q1, output signal can also be taken from the emitter, in addition to the output  $V_{o1}$  taken from the collector. According to the characteristics of emitter follower, the output signal from the emitter is in same phase with, and in approximately same magnitude with ( $A_v \approx 1$ ), the input signal of the base. The signal exhibited at the emitter of Q1 is therefore in same phase with and in approximately same magnitude with  $V_{i1}$ .

Because the emitters of Q1 and Q2 are connected together, the emitter of Q2 relative to ground also exhibits the signal same as the emitter of Q1 with the magnitude that is approximately equal to  $V_{i1}$  and with the same phase.

The emitter signal of Q2 exhibits between emitter and ground, while the base of Q2 is directly connected to ground. This signal, which is virtually applied between emitter and base, can be viewed as the input signal of Q2. The signal relative to the base of Q1 is in inverse phase with  $V_{i1}$ . In other words, the signal applied to the base of Q2 is in inverse phase with but in same magnitude with  $V_{i1}$ .

The signal applied to the base of Q2, that is in inverse phase but in same magnitude with  $V_{i1}$ , is amplified by Q2, and then the output signal  $V_{o2}$  will be delivered from the collector. Because the base signal of Q2 is in inverse phase with  $V_{i1}$ , and also because  $V_{o2}$  is in inverse phase with this base signal since the output signal from the collector shall be in inverse phase with the base signal,  $V_{o2}$  is therefore in same phase with  $V_{i1}$ , as shown in Fig 14.4 (b). If the voltage gains for both Q1 and Q2 are  $A_v$ ,  $V_{o2} = V_{o1}$  but with inverse phase since the magnitude of Q2 base signal is equal to the input signal  $V_{i1}$  applied to the Q1 base, which can be expressed as  $V_{o2} = A_v V_{i1}$ .

In summary, if the input signal is applied to  $V_{i1}$ , an amplified signal with inverse phase will be obtained from  $V_{o1}$ , and an amplified signal with same phase will be obtained from  $V_{o2}$ , wherein the magnitude of  $V_{o1}$  is same as that of  $V_{o2}$ , as shown in Fig 14.5 (a). If the input signal is applied to  $V_{i2}$ , an amplified signal with inverse phase will be obtained from  $V_{o2}$ , and an amplified signal with same phase will be obtained from  $V_{o1}$ , as shown in Fig 14.5 (b).

If the input signal is applied to either one of the input terminals of the differential amplifier with single-end input, the amplified signals with same magnitude and inverse phase can be obtained from  $V_{o1}$  and  $V_{o2}$ .

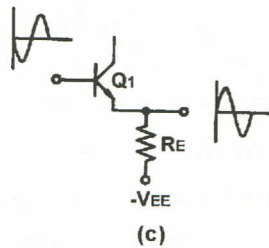
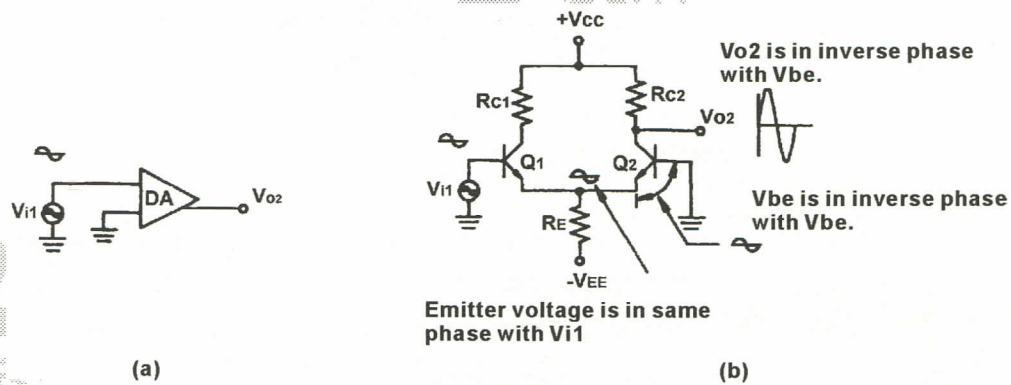


Fig 14.4 Single-end input, single-end output ( II )

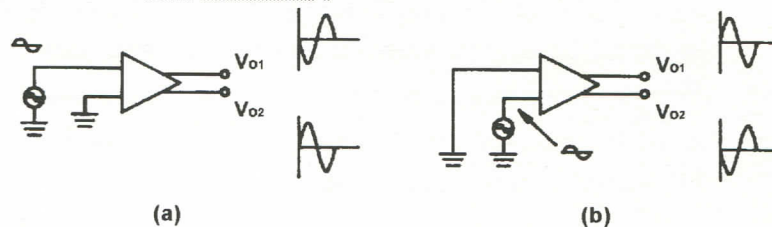
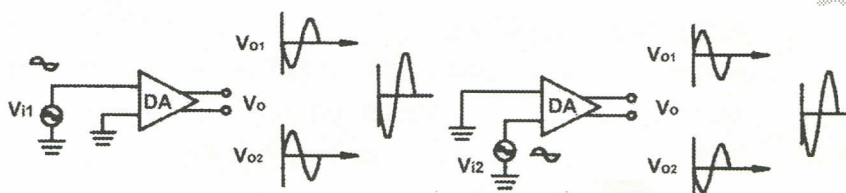


Fig 14.5 Output signal of the OP AMP with single-end input

## 2) Single-end input, dual-end output



$$V_o = V_{o1} - V_{o2} = 2V_{o1} = -2A_v V_{i1} \text{ or } 2A_v V_{i2}$$

Fig 14.6

## 3) Dual-end input, single-end output

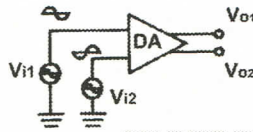


Fig 14.7

As shown in Fig 14.7

$$V_{o1} = -A_v V_{i1} + A_v V_{i2} = -A_v (V_{i1} - V_{i2}) \quad \text{--- 14-1.1}$$

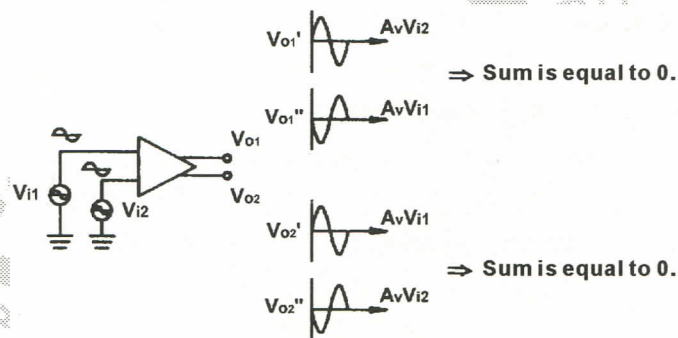
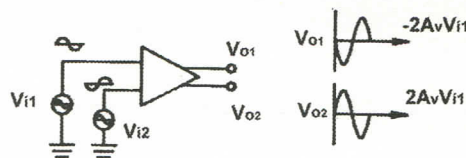
$$\begin{aligned} V_{o2} &= A_v V_{i1} + (-A_v V_{i2}) = A_v V_{i1} - A_v V_{i2} \\ &= A_v (V_{i1} - V_{i2}) \quad \text{--- 14-1.2} \end{aligned}$$

$$V_d = V_{i1} - V_{i2} = V_{i1} - (-V_{i1}) = 2V_{i1} \text{ or } V_d = -2V_{i1}$$

From Equation 14-1.1 and 14-1.2 we can find out:

① If  $V_{i1} = V_{i2}$  (same phase),  $V_{o1} = 0$  and  $V_{o2} = 0$ , as shown in Fig 14.8.

② If  $V_{i1} = -V_{i2}$  (inverse phase),  $V_{o1} = -2A_v V_{i1}$  and  $V_{o2} = 2A_v V_{i1}$ , as shown in Fig 14.9.

Fig 14.8 The waveforms of  $V_{o1}$  and  $V_{o2}$  when  $V_{i1} = V_{i2}$  (same phase)Fig 14.9 The waveforms of  $V_{o1}$  and  $V_{o2}$  when  $V_{i1} = -V_{i2}$



## 4) Dual-end input, dual-end output

As shown in Fig 14.8 and 14.9,

$$\begin{aligned} V_o &= V_{o1} - V_{o2} = -A_v (V_{i1} - V_{i2}) - A_v (V_{i1} - V_{i2}) \\ &= -2A_v (V_{i1} - V_{i2}) = -2A_v V_d \end{aligned}$$

If ①  $V_{i1} = V_{i2}$ ,  $V_o = 0$

②  $V_{i1} = -V_{i2}$ ,  $V_o = -2A_v (2V_{i1}) = -4A_v V_{i1}$

## (3) Gain of differential amplifier

**Ac** : Common mode gain; means the amplification factor with respect to the same signal.

**Ad** : Differential mode gain; means the amplification factor with respect to the differential signal.

**Vc** : Common mode signal (same signal).

**Vd** : Differential mode signal (differential signal).

$$V_o = A_d V_d + A_c V_c$$

The value of  $A_c$  in an ideal differential amplifier shall be as smaller as possible, and the value of  $V_o$  shall be directly proportional to  $A_d$ .

## (4) CMRR : Common Mode Rejection Ratio

CMRR =  $A_d/A_c$  is used to indicate the capability of a differential amplifier (or an OP AMP) to compress the noise. The larger CMRR value, which corresponds to the smaller  $A_c$  value, represents the better capability to compress the noise.

$$\begin{aligned} \text{And } V_o &= A_d V_d + A_c V_c = A_d V_d + A_d V_d \times \frac{A_c V_c}{A_d V_d} = A_d V_d \left( 1 + \frac{V_c}{V_d} \times \frac{A_c}{A_d} \right) \\ &= A_d V_d \left( 1 + \frac{1}{\text{CMRR}} \times \frac{V_c}{V_d} \right) \end{aligned}$$

This can also explain when CMRR is larger,

$$V_o = A_d V_d \left( 1 + \frac{1}{\text{CMRR}} \times \frac{V_c}{V_d} \right) = A_d V_d (1 + 0) = A_d V_d$$

The common mode signal is thus compressed. Because the noises are typically exist in  $V_{i1}$  and  $V_{i2}$  simultaneously like common mode signal, the differential amplifier with larger CMRR value will own the better capability to compress the noise. The CMRR values can be looked up from the DA and OP AMP specification manuals.

## 14-2 Basic characteristics of OP AMP

### (1) What is OP AMP?

1. The OP AMP is an IC called Operational Amplifier, which can also called OPA as abbreviation.
2. OPA is the amplifier including one inverting input terminal (-), one noninverting input terminal (+) and one output terminal,

with symbol shown in Fig 14.10.



Fig 14.10

3. OPA typically incorporates two power supplies with same magnitude and different polarities, usually  $\pm 3V \sim \pm 24V$  wherein  $\pm 12V$  is most widely used. The connection is shown in Fig 14.11.

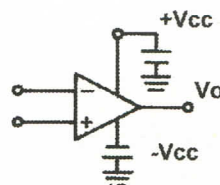


Fig 14.11

The internal equivalent circuit of the OP AMP is shown in Fig 14.1 (the example of 741), which is very similar to OCL AMP. If  $V_i = 0V$ ,  $V_o$  will be  $0V$ . Single power supply can also be incorporated in the OP AMP, and at this time  $V_o$  will be  $1/2 V_{cc}$  instead of  $0V$  if  $V_i$  is applied.

(2) The ideal OP AMP shall own the following characteristics:

1.  $A_v = \infty$
2.  $Z_i = \infty$
3.  $Z_o = 0$
4.  $BW = \infty$
5. If  $V_i = 0$ ,  $V_o = 0$ .
6. The characteristics in insensitive to the temperature.

We will introduce the widely used characteristic parameters as follows:

1)  $Z_i$ : Input Impedance

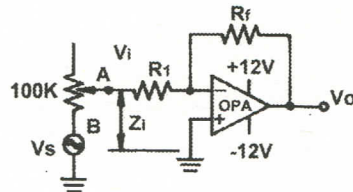
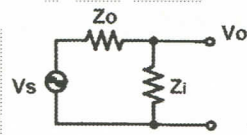


Fig 14.12

The ideal value of the OP AMP itself is  $\infty$ , the actual value is also very large. However, after various circuits have been connected,  $Z_i$  shall include the effect of peripheral parts ( $R_1$  and  $R_f$ ), as shown in Fig 14.12. The  $Z_i$  shown in Fig 14.12 is calculated using the concept of load effect.



$$\text{If } V_o = \frac{1}{2} V_s, Z_i = Z_o$$

2)  $Z_o$ : Output Impedance

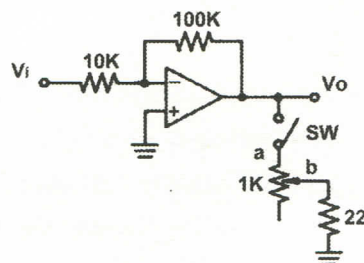
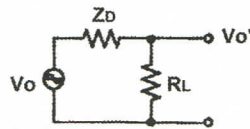


Fig 14.13

The method to calculate  $Z_o$  in Fig 14.13 is same as that to calculate  $Z_i$ . As shown in the following Fig, If  $R_L = \infty$



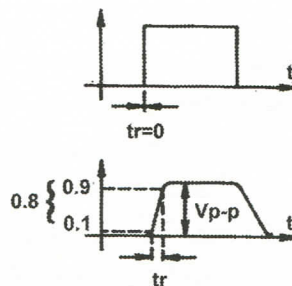


When  $V_o' = V_o$  and  $Z_o = R_L$ ,  $V_o' = 1/2 V_o$ .

As shown in Fig 14.13, we can first adjust VR1K so that  $V_o' = 1/2 V_{cc}$ , then measure the value of  $R_L$  ( $VR1Kab + 22\Omega$ ), which is  $Z_o$ . If  $V_o' = 1/2 V_{cc}$  can not be adjusted, we can also use the equation of voltage divider  $V_o' = \frac{R_L}{Z_o + R_L} V_o$  to calculate  $Z_o$ .

Then setting  $R_L = \infty$ , the  $V_o$  can be measured.

### 3) SR: Slew Rate $0.8V_{p-p} / tr$



rise time

Fig 14.14

As shown in Fig 14.14, we can understand that SR is used to indicate the signal transmission speed by the OPA. Larger SR corresponds to the quicker transmission speed of the signal, also representing the higher capability to handle the high-frequency signal. In general, larger SR also corresponds to the wider BW.

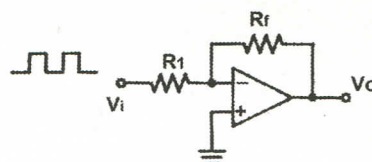


Fig 14.15

The circuit for measuring SR is shown in Fig 14.15. The  $t_r$  and  $V_{p-p}$  can be calculated from the waveform of  $V_o$ . Then the SR can be calculated using the equation  $SR = 0.8V_{p-p}/t_r$ , where  $0.8V_{p-p}$  represents the change magnitude of the voltage during rise time, and  $t_r$  represents the rise time.

#### 4) BW: Bandwidth

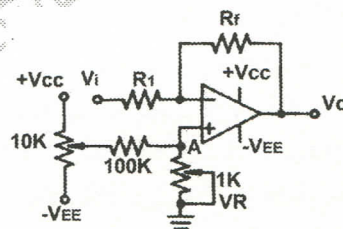
The BW of an ideal OPA will be up to  $\infty$ , but it is not the real case. The value of BW listed in the typical specification manual is above a few MHz. However, what's the BW for the commercially available IC? The experiment shown in Fig 14.16 can tell us the results. In practice, if the BW value is too low, it is not suitable for the high frequency circuit.

#### 5) Offset Voltage (zero level adjustment)

The  $V_o$  shall be 0V for an ideal OPA if  $V_i = 0$ , but it is not so ideal in practice because  $V_o$  is usually not 0V if  $V_i = 0$ .

If this OPA is utilized in the control circuit, the operation state will be affected if  $V_o \neq 0$  when  $V_i = 0$ . Utilizing the offset voltage adjustment, which will result in  $V_o = 0V$  when  $V_i = 0V$ , must be carried out in the practical circuit. The offset voltage adjustment can be classified into the following methods.

##### 1. Offset in the inverting amplification side



$$V_o = V_i \left( -\frac{R_f}{R_1} \right)$$

Fig 14.16

When  $V_i = 0V$ , adjust  $1K\Omega$   $VR$  so that  $V_o = 0V$ .

Because  $V_o = V_a (1 + R_f/R_1)$  when  $V_i$  is connected to ground, the adjustment of  $VR$   $1K\Omega$  and  $VR$   $100K\Omega$  can change the value of  $V_o$ .

## 2. Offset in the noninverting amplification side

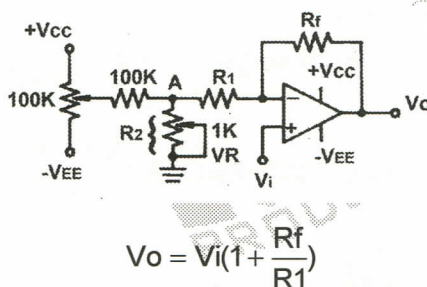


Fig 14.17

Because  $A_v = -\frac{R_f}{R_1 + R_2}$ ,  $R_2$  shall be much less than  $R_1$

so that  $A_v \approx -R_f/R_1$ .

Because  $V_o = V_a (-R_f/R_1)$  when  $V_i = 0$  (connected to ground), the adjustment of  $VR1K\Omega$  and  $VR100K$  can change the value of  $V_o$ .

## 3. Offset in voltage follower

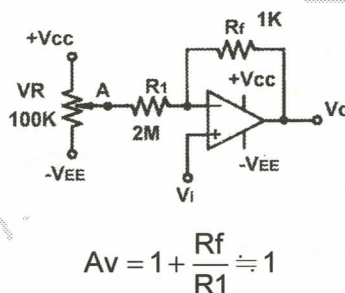


Fig 14.18

Because  $V_o = V_a (-R_f/R_1)$  when  $V_i = 0$  (connected to ground), the adjustment of  $VR100K$  can change the value of  $V_o$ .

## 4. Built-in offset in OPA

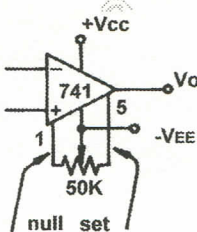


Fig 14.19



The circuit shown in Fig 14.19 can be connected by utilizing the built-in offset null set of the IC, then the  $V_o$  value can be improved by adjusting the balance status of the internal differential stage of the IC.

### 14.3 Experiment Equipments:

- (1) KL-200 Linear Circuit Lab.
- (2) Experiment Module: KL-23012.
- (3) Experiment Instrument :
  1. Voltmeter.
  2. Oscilloscope.
  3. Signal generator.
- (4) Tools: Basic hand tools.
- (5) Materials: As indicated in the KL-23012.

### 14.4 Experiment Items:

Item one (14-1): Transistor differential amplifier circuit 14-1-1

#### 14-1-1-1 Experiment Procedures:

- (1) Insert the short-circuit clip by referring to Fig 14-20 and the short-circuit clip arrangement diagram 23012-block c.
- (2) Connect the signal generator and oscilloscope to the input terminal, then connect the oscilloscope to the output terminal.
- (3) Adjust VR1 so that the resistance at points B and C will be the maximum ( $V_{in1} = V_{in2}$ ).
- (4) Adjust the output of the signal generator to 1KHz, then increase the amplitude so that the maximum non-distorted waveform of the output terminal can be displayed. Measure  $IN_1$ ,  $IN_2$ ,  $OUT_1$  and  $OUT_2$  respectively, and record the waveforms.

(5) Adjust VR1 so that the resistance at points B and C will be the minimum ( $0\Omega$ ) and  $V_{IN2} = 0V$ .

(6) Repeat Step (4).

(7) Adjust VR1 so that the resistance at points B and C will be  $500\Omega$  and  $V_{IN2} = 1/2 V_{IN1}$ .

(8) Repeat Step (4).

#### 14-1-1-2 Experiment Result:

The experiment results shall be recorded in Table 14-1.














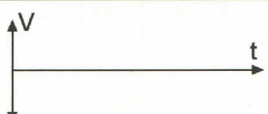

	$V_{IN1}=V_{IN2}$	$V_{IN2}=0V$	$V_{IN2}=1/2V_{IN1}$
$V_{IN1}$			
$V_{IN2}$			
$V_{OUT1}$			
$V_{OUT2}$			
$V_{OUT}$			

Table 14-1

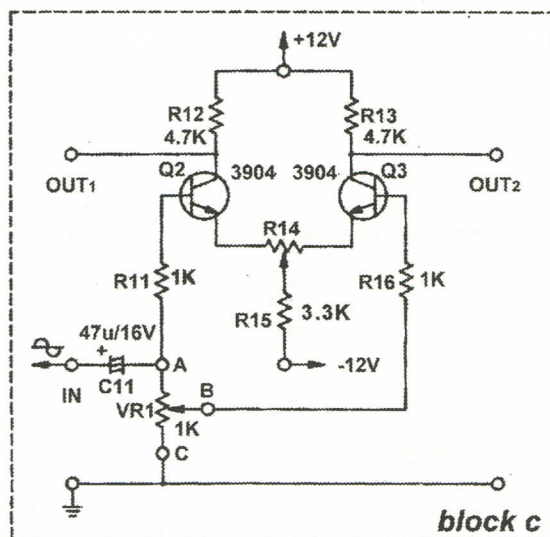


Fig. 14-20 (Fig 23012-block c)

Item two (14-2): Experiment for the basic characteristics of OP AMP –  $Z_i$ ,  $Z_o$ , SR, BW and offset

### 14-2-1 Experiment for $Z_i$

#### 14-2-1-1 Experiment Procedures:

- (1) Insert the short-circuit clip by referring to Fig 14-21 (a) and the short-circuit clip arrangement diagram 23012-block d.1.
- (2) Adjust the output of the signal generator to 1KHz sine wave, then adjust the output amplitude to the minimum.
- (3) Adjust VR100K (VR3) to the minimum (at which the point B and point C will be connected).
- (4) Adjust the amplitude so that the maximum non-distorted waveform of OUT will be displayed.
- (5) View and record the waveform of IN.
- (6) Adjust VR until the signal in the input terminal (IN) is one half of the waveform in Step (4).
- (7) Turn off the power supply.
- (8) Use the multimeter ( $\Omega$  scale) to measure the resistance value between B and C of VR 100K. This value is the  $Z_i$  of OP AMP.



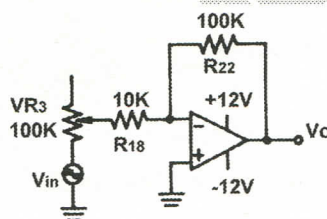
**14-2-1-2 Experiment Result:** $Z_i = \underline{\hspace{2cm}}$ .

Fig 14-21 (a)

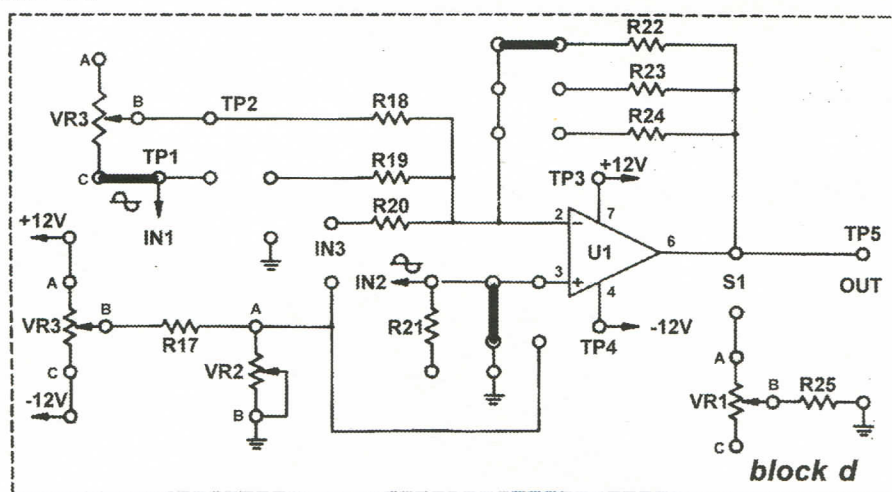


Fig 23012-block d.1

**14-2-2 Experiment for  $Z_o$** **14-2-2-1 Experiment Procedures:**

- (1) Insert the short-circuit clip by referring to Fig 14-21 (b) and the short-circuit clip arrangement diagram 23012-block d.2.
- (2) Adjust the output of the signal generator to 1KHz sine wave.
- (3) Turn off SW1.
- (4) Adjust the signal generator so that the maximum non-distorted waveform of  $V_{out}$  will be displayed.
- (5) Record the  $V_{p-p}$  value of  $V_{out}$ .

- (6) Turn on SW1, then view the waveform variation of Vout.
- (7) Adjust VR1K $\Omega$  (VR1) until Vout is one half of that in Step (5).
- (8) Turn off the power supply.
- (9) Use the multimeter ( $\Omega$  scale) to measure the resistance value of output terminal relative to ground. This value is the output impedance of the OP AMP.
- (10) Adjust the signal generator to different frequencies of 100 Hz, 10KHz and 50KHz, then repeat Step (2) to (9). Check if the output impedance will be changed with the signal frequency.

#### 14-2-2-2 Experiment Result:

The experiment results shall be recorded in Table 14-2 (a).

	Zo
1KHz	
100Hz	
10KHz	
50KHz	

Table 14-2 (a)

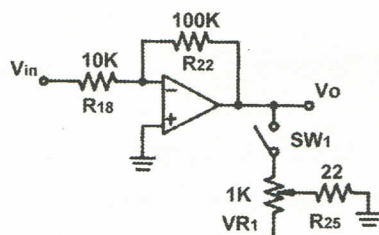


Fig 14-21 (b)

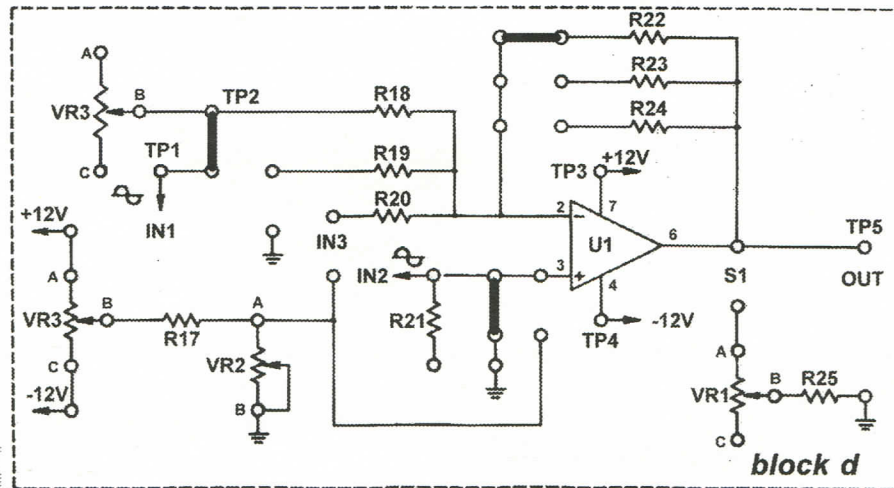


Fig 23012-block d.2

### 14-2-3 Experiment for SR (Slew Rate)

#### 14-2-3-1 Experiment Procedures:

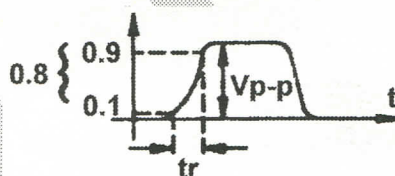
- (1) Insert the short-circuit clip by referring to Fig 14-21 (c) and the short-circuit clip arrangement diagram 23012-block d.3.
- (2) Connect the signal generator to the input terminal (IN1), then adjust the output of the signal generator to 1KHz square wave.
- (3) Connect the oscilloscope to the output terminal.
- (4) Adjust the frequency of input signal until the rise wave of the output signal can be measured by the oscilloscope. View  $V_{p-p}$  and  $t_r$ .

#### 14-2-3-2 Experiment Result:

SR can be calculated from the following Equation

$SR = 0.8V_{p-p} / t_r$ , where  $t_r$  represents the rise time.

$t_r$ : rise time





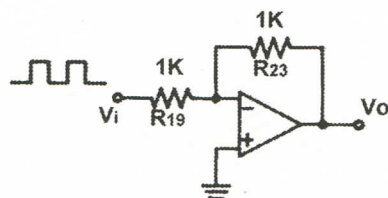


Fig 14-21 (c)

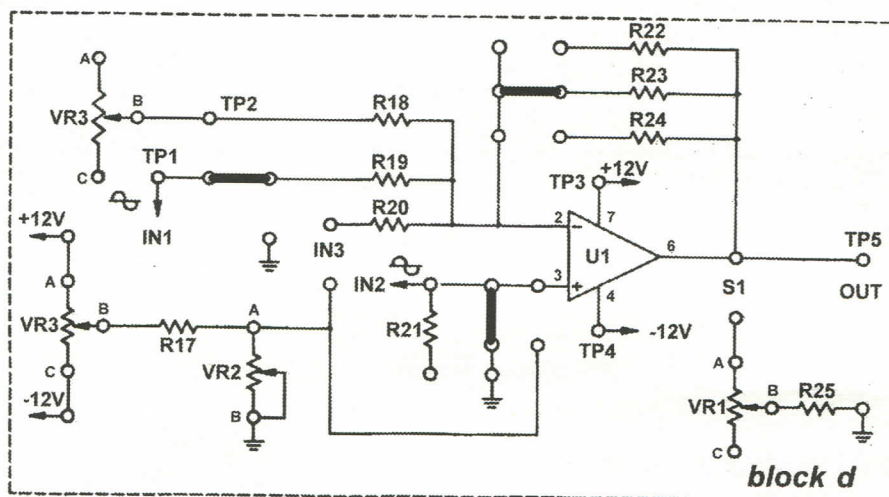


Fig 23012-block d.3

## 14-2-4 Experiment for BW (Band Width)

### 14-2-4-1 Experiment Procedures:

- (1) Insert the short-circuit clip by referring to Fig 14-21 (d) and the short-circuit clip arrangement diagram 23012-block d.4. Apply 1K Hz sine wave to the input terminal.
- (2) As indicated in Table (1), increase the input voltage from 50mVp-p to 200mVp-p, then view the output waveform, and make records.

Table (1)

Vi	50m Vp-p	Vo	Vp-p	AV	
Vi	100m Vp-p	Vo	Vp-p	AV	
Vi	200m Vp-p	Vo	Vp-p	AV	

- (3) Increase the input voltage so that the maximum non-distorted waveform of output terminal can be displayed.

- (4) Adjust the input voltage to 100mVp-p.
- (5) Change the frequency from 50Hz to 30KHz as indicated in Table (2), then measure the corresponding output voltage.

Table (2)

f (Hz)	V <sub>o</sub>	A <sub>v</sub>	A <sub>v</sub> (db)	f (Hz)	V <sub>o</sub>	A <sub>v</sub>	A <sub>v</sub> (db)
50				5000			
200				10000			
500				12000			
1000				15000			
2000				30000			

- (6) Plot the curve of gain versus frequency response in the coordinate paper with vertical coordinate representing db and horizontal coordinate representing frequency, then mark the point of -3db.

**14-2-4-2 Experiment Result:**

Plot the curve of gain versus frequency response in Table 14-3, with vertical coordinate representing db and horizontal coordinate representing frequency, then mark the point of -3db.

A<sub>vo</sub>: The A<sub>v</sub> when V<sub>o</sub> is the maximum



Table 14-3

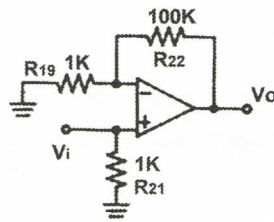


Fig 14-21 (d)

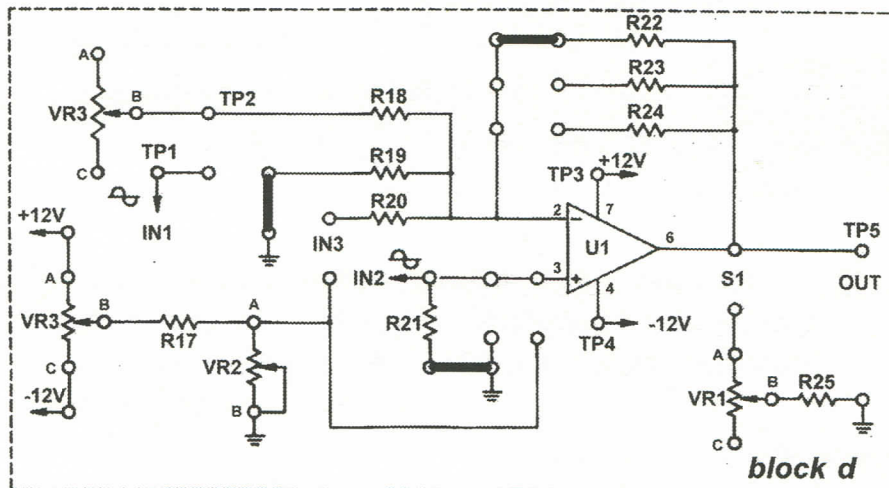


Fig 23012-block d.4

### 14-2-5 Offset voltage adjustment in the amplifier with inverting configuration

#### 14-2-5-1 Experiment Procedures:

- (1) Insert the short-circuit clip by referring to Fig 14-21 (e) and the short-circuit clip arrangement diagram 23012-block d.5.
- (2) Connect the inverting input terminal (IN3) of the OP AMP to ground.
- (3) Use oscilloscope (DCV) or voltmeter (DCV) to measure the voltage in the output terminal (OUT).
- (4) View if the voltage in OUT is zero. If not, please
  - ① Adjust VR2 (VR1K) to the maximum.
  - ② Adjust VR3 (VR100K) and view the voltage variation of OUT, so that  $V_{out} = 0V$ .



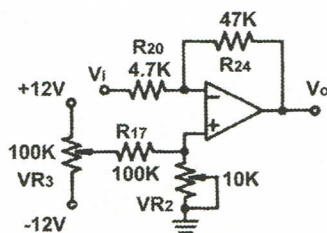


Fig 14-21 (e)

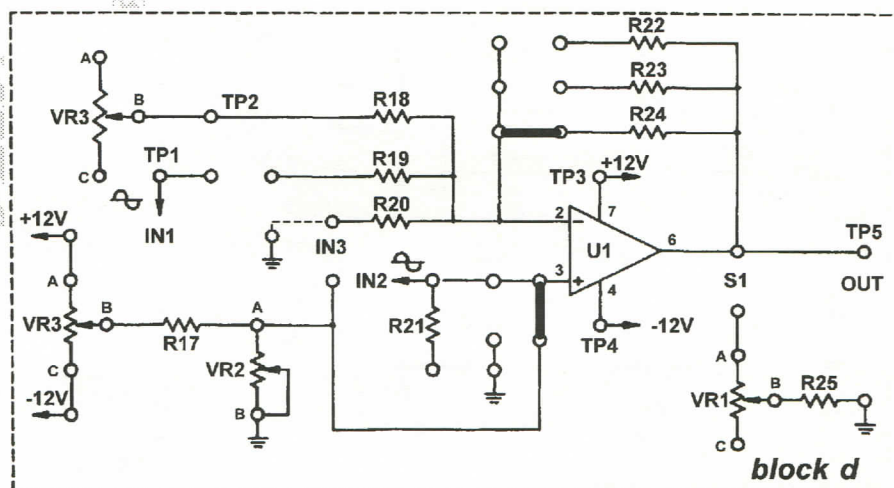


Fig 230012-block d.5

### 14-2-6 Offset voltage adjustment in the amplifier with noninverting configuration

#### 14-2-6-1 Experiment Procedures:

- (1) Insert the short-circuit clip by referring to Fig 14-21 (f) and the short-circuit clip arrangement diagram 23012-block d.6.
- (2) Connect the noninverting input terminal (IN2) of the OP AMP to ground.
- (3) Use oscilloscope (DCV) or voltmeter (DCV) to measure the voltage in the output terminal (OUT).
- (4) View if the voltage in OUT is zero. If not, please
  - ① Adjust VR2 (VR1K) to the maximum.
  - ② Adjust VR3 (VR100K) and view the voltage variation of OUT, so that  $V_{out} = 0V$ .

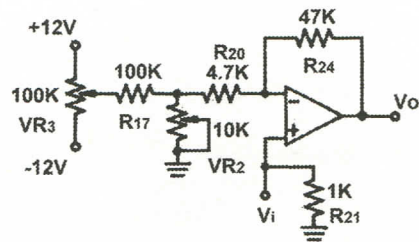


Fig 14-21 (f)

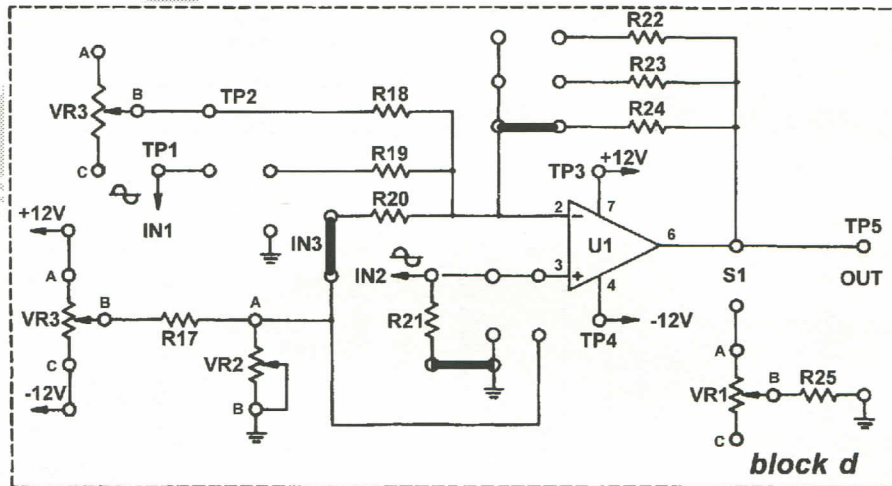


Fig 230012-block d.6

## 14.5 Experiment Discussion:

The characteristic parameters of the OPA listed in the specification manual include:

- (1) Input Offset Voltage (mV).
- (2) Average Input Offset Voltage Drift ( $\mu\text{V}/^\circ\text{C}$ ).
- (3) Input Offset Current (nA).
- (4) Average Input Offset Current Drift ( $\text{nA}/^\circ\text{C}$ )
- (5) Input Bias Current.
- (6) Power supply Rejection Ratio ( $\mu\text{V/V}$ ).
- (7) Output Short Circuit Current (mA).
- (8) Power Dissipation (mW).
- (9) Input Impedance ( $\text{M}\Omega$ ).
- (10) Bandwidth (MHz).
- (11) Slew Rate: The change rate of the output voltage ( $\text{V}/\mu\text{S}$ ).
- (12) CMRR: Common Mode Rejection Ratio (db).
- (13) Output Impedance ( $\text{M}\Omega$ ).

The symbols in the ( ) represent the units.

Only the experiments of some most frequently used parameters are carried out in this unit.

### (a) $Z_i$

The  $Z_i$  listed in the specification manual, for the example of  $\mu\text{A}741$ , is  $10\text{M}\Omega$ . However, when the OPA is used as the amplifier with inverting configuration, the impedance of the overall circuit will be decreased due to the effect of negative feedback circuit. If the amplifier circuit with high input impedance is required, the amplifier with noninverting configuration or cascade with voltage follower can be adopted.

### (b) $Z_o$

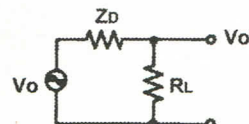
Considering the  $Z_o$  of the OPA which is typically a few  $\Omega$ , if the load resistance value is also very small, the output of the OPA will be easily saturated, and the waveform will be clipped off. If the voltage divider method is adopted to measure the  $Z_o$ , the resistor with larger resistance value shall be connected as load to prevent the  $V_o$  from distortion.

Voltage divider method:

When  $R_L = \infty$ ,  $V_o' = V_o$ .

When  $R_L \neq \infty$ , we can get

$$V_o' = V_o \frac{R_L}{Z_o + R_L}$$





where  $V_o'$  can be measure by voltmeter,  $R_L$  value is already known, and  $V_o$  value is already known.

$Z_o$  can thus be calculated.

(c) BW

The value of BW listed in the specification manual may be up to a few MHz. However, the actually measured values can not coincide with the specification, but can only reach a few hundreds KHz. Especially the BW's of the IC's sold by components reseller stores hardly reach a few MHz.

(d) Measurement of offset voltage

The voltage adjustment carried out in the preserved null offset (such as the pin 1.5 of 741) of the input terminal or IC to compensate the output DC level of the OPA so that 0V output will be delivered during static state is called offset voltage adjustment. Because the typical output offset voltage is around  $\pm 1V$ , feeding  $\pm 10mV$  in the input terminal, if the amplification factor 100 for the inverting amplifier is assumed, can offset the output  $\pm 1V$  to 0V. Because the open loop gain of OPA is approximately  $\infty$ , the offset voltage adjustment for the comparator is very difficult.  $+V_{cc}$  or  $-V_{cc}$  is therefore used as the output instead of 0V output.

## 14.6 Problems:

### (1) Selection:

( ) 1. Which configuration is adopted in the input stage of the OPA:

1. push-pull amplifier.
2. differential amplifier.
3. CB amplifier.

( ) 2.  $Z_i$  of the OPA in the ideal case shall be:

1.  $\infty$
2.  $1\text{M}\Omega$
3.  $0\Omega$

( ) 3.  $Z_o$  of the OPA in the ideal case shall be: frequency of FM is:

1.  $\infty$
2.  $1\text{M}\Omega$
3.  $0\Omega$

( ) 4. For the bandwidth of the OPA, which is correct among the following descriptions:

1.  $0\text{Hz} \sim \text{a few MHz}$ .
2. only a few KHz.
3. low frequency response is very poor.

( ) 5. For an ideal OPA, when  $V_i = 0$ ,

1.  $V_o = +V_{cc}$
2.  $V_o = 1\text{V}$
3.  $V_o = 0\text{V}$

## (2) Practice:

1. Please repeat the basic characteristic experiment described in 14-2 by using the OPA's with three different Type No. (such as  $\mu$ A741, LM301,  $\mu$ A709 ... etc.), then describe the advantages and disadvantages among them.
2. Look up linear IC data book, or OPA specification manual, or the Appendixes of this Manual, then record the IC data of the following Table.

Type No.	Power Supply Range	Zi	Zo	BW	CMRR	Av	Slew Rate
LM301							
$\mu$ A709							
$\mu$ A741							
$\mu$ A747							
LM324							
LM380							
LM387							
LM3900							